COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4047B

PRELIMINARY DATA

LOW-POWER MONOSTABLE/ASTABLE MULTIVIBRATOR

- LOW POWER CONSUMPTION: SPECIAL COS/MOS OSCILLATOR CONFIGURATION
- MONOSTABLE (ONE-SHOT) OR ASTABLE (FREE-RUNNING) OPERATION
- TRUE AND COMPLEMENTED BUFFERED OUTPUTS
- ONLY ONE EXTERNAL R AND C REQUIRED
- BUFFERED INPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4047B** (extended temperature range) and **HCF 4047B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4047B** consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options. Inputs include +TRIGGER, - TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$, and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals. For operating modes see functional terminal connections and application notes.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

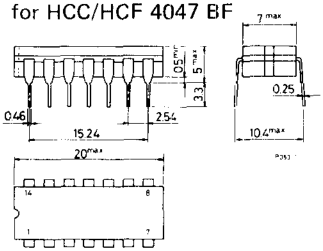
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

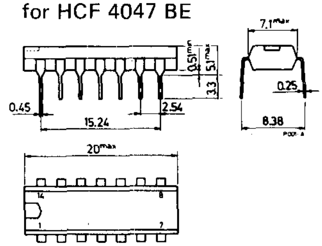
HCC 4047 BD	for dual in-line ceramic package
HCC 4047 BF	for dual in-line ceramic package, frit seal
HCC 4047 BK	for ceramic flat package
HCF 4047 BE	for dual in-line plastic package
HCF 4047 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

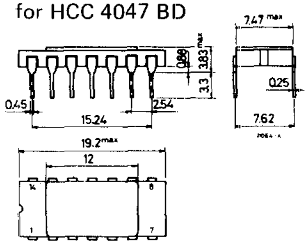
Dual in-line ceramic package
for HCC/HCF 4047 BF



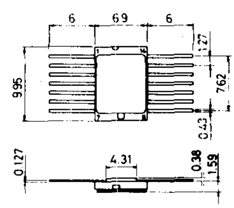
Dual in-line plastic package
for HCF 4047 BE



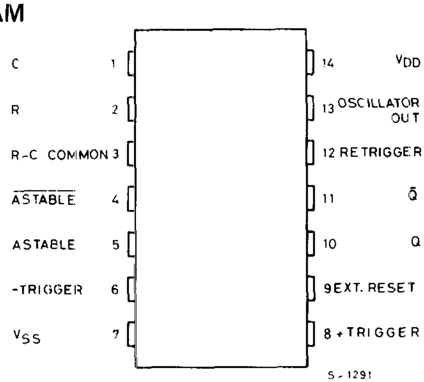
Dual in-line ceramic package
for HCC 4047 BD



Ceramic flat package
for HCC 4047 BK



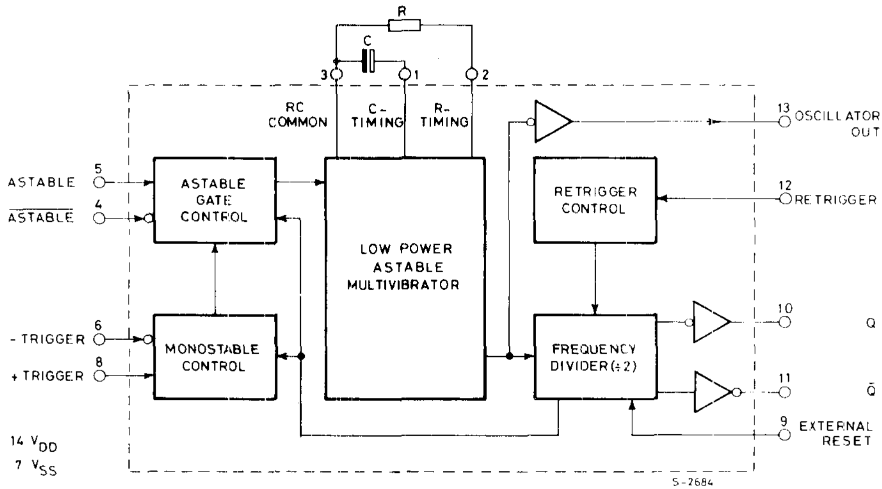
CONNECTION DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

BLOCK DIAGRAM

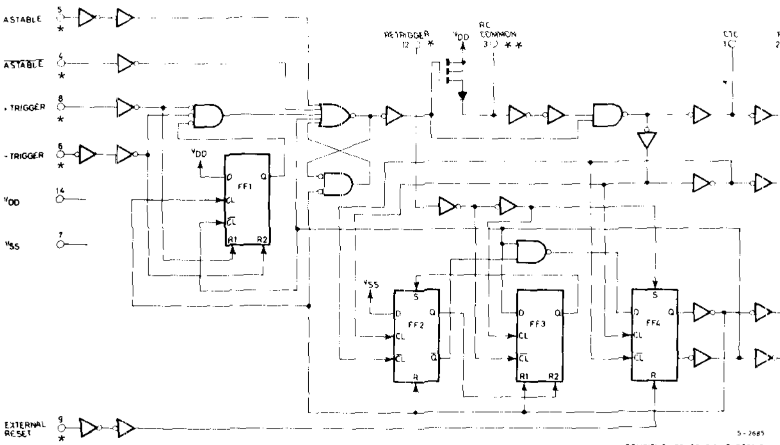


FUNCTIONAL TERMINAL CONNECTIONS

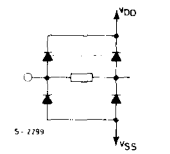
FUNCTION*	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	t_A (10, 11) = 4.40 RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A (13) = 2.20 RC
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator:					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M (10, 11) = 2.48 RC
External Countdown**	14	5, 6, 7, 8, 9, 12	–	10, 11	

* In all cases external capacitor and resistor between pins, 1, 2 and 3 (see logic diagrams)
** Input pulse to Reset of External Counting Chip
External Counting Chip Output to pin 4

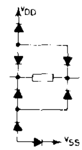
LOGIC DIAGRAM



CAUTION: PIN 3 IS MORE SENSITIVE TO STATIC ELECTRICAL DISCHARGE. EXTRA HANDLING PRECAUTIONS ARE RECOMMENDED



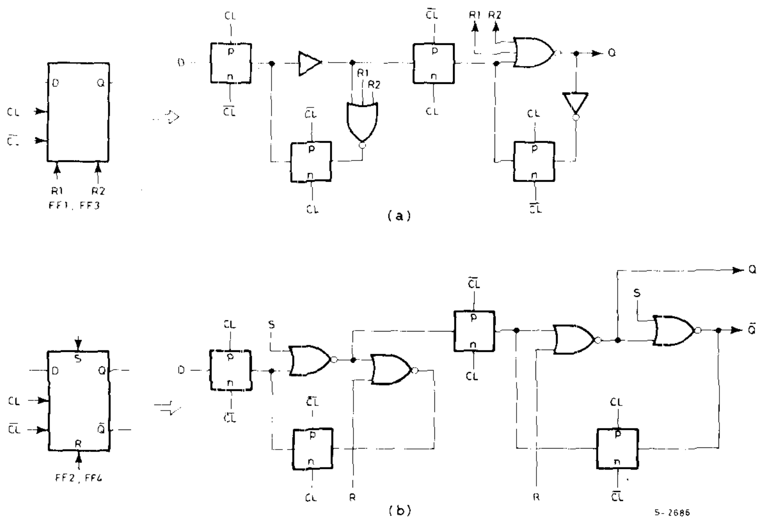
* ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK



** SPECIAL RC COMMON PROTECTION NETWORK

5-2683

Detail for flip-flops FF1 and FF3 (a) and for flip-flops FF2 and FF4 (b)



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	V_{DD} (V)	Values T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	µA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	µA
C_I**	Input capacitance									5	7.5			pF

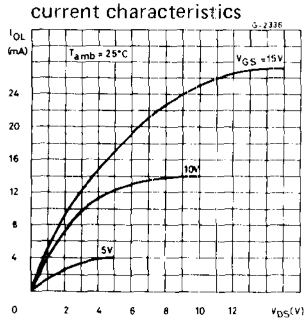
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS

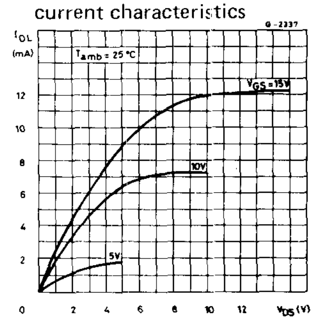
(T_{amb} = 25°C, C_L = 15 pF, R_L = 200 KΩ typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter			Test conditions	V_{DD} (V)	Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL}	Propagation delay time	Astable, $\overline{\text{Astable}}$ to osc. out.		5		200		ns
				10		100		
				15		70		
		Astable, $\overline{\text{Astable}}$ to Q, $\overline{\text{Q}}$		5		550		
				10		250		
				15		150		
		+Trigger, −Trigger to Q, $\overline{\text{Q}}$		5		700		
				10		300		
				15		200		
		+Trigger, Retrigger to Q, $\overline{\text{Q}}$		5		300		
				10		175		
				15		125		
		External Reset to Q, $\overline{\text{Q}}$		5		300		
				10		125		
				15		75		
t_{THL}, t_{TLH}	Transition time osc. out Q, $\overline{\text{Q}}$			5		100		ns
				10		50		
				15		40		
t_W	Input pulse width (any input)			5		500		ns
				10		200		
				15		140		
t_r, t_f	+Trigger, Retrigger rise and fall time			5		15		µs
				10		5		
				15		5		

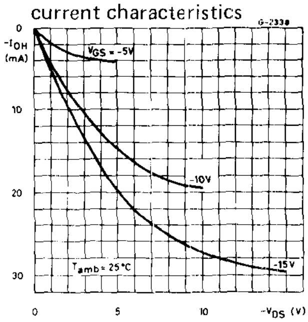
Typical output low (sink) current characteristics



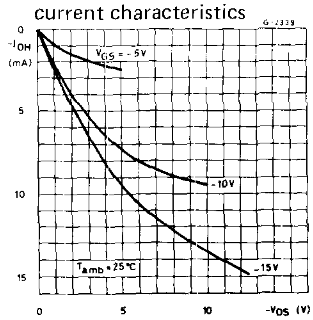
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

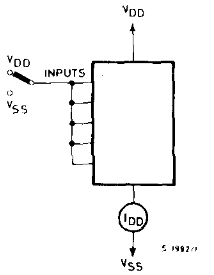


Minimum output high (source) current characteristics

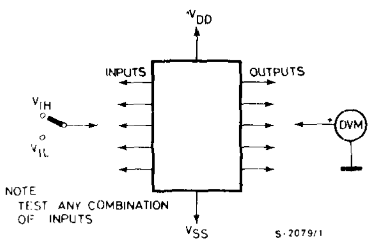


TEST CIRCUITS

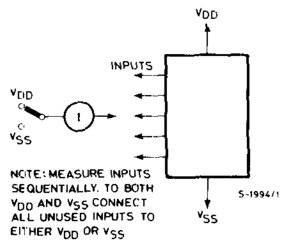
Quiescent device current



Input voltage



Input current



APPLICATION INFORMATION

1 - Circuit description

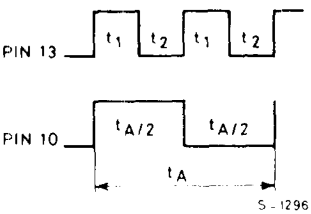
Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output. In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the -TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the -TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components. An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

APPLICATION INFORMATION (continued)

2 - Astable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% - 67% V_{DD}) for free-running (astable) operation.

Astable mode waveforms



$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2 V_{DD} - V_{TR}}$$

$$t_A = 2 (t_1 + t_2) = -2 RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2 V_{DD} - V_{TR})}$$

Typ : $V_{TR} = 0.5 \ V_{DD}$ $t_A = 4.40$ RC
Min : $V_{TR} = 0.33 \ V_{DD}$ $t_A = 4.62$ RC
Max : $V_{TR} = 0.67 \ V_{DD}$ $t_A = 4.62$ RC

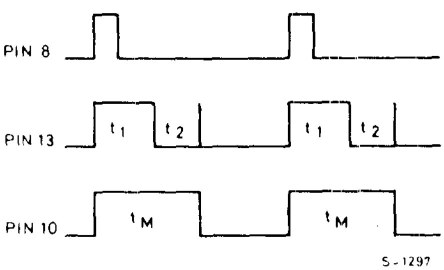
thus if $\boxed{t_A = 4.40 \text{ RC}}$ is used, the maximum variation will be (+5,0%, -0.0%)

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature.

3 - Monostable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% - 67% V_{DD}) for one-shot (monostable) operation.

Monostable waveforms



$$t_1 = -RC \ln \frac{V_{TR}}{2 V_{DD}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2 V_{DD} - V_{TR}}$$

$$t_M = (t_1 + t_2) = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2 V_{DD} - V_{TR})(2 V_{DD})}$$

APPLICATION INFORMATION (continued)

where t_M = monostable mode pulse width. Values for t_M are as follows:

Typ : $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min : $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max : $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

Thus if $\boxed{t_M = 2.48\ RC}$ is used, the maximum variation will be (+9.3%, -0.0%).

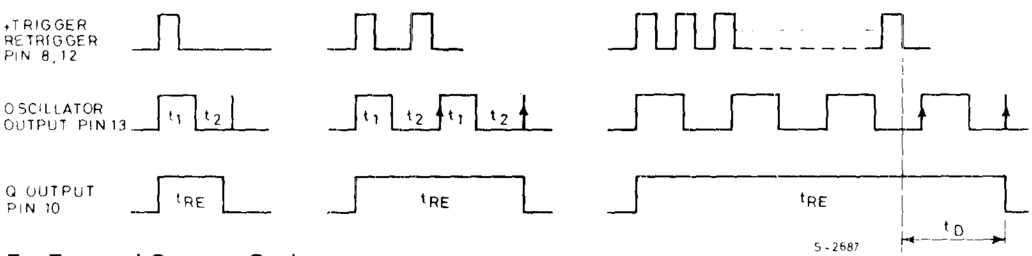
Note: In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature.

4 - Retrigger Mode

The **HCC/HCF 4047B** can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. A normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT) terminates at some variable time t_D after the termination of the last retrigger pulse. t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see logic diagram).

Fig. A - Retrigger-mode waveforms



5 - External Counter Option

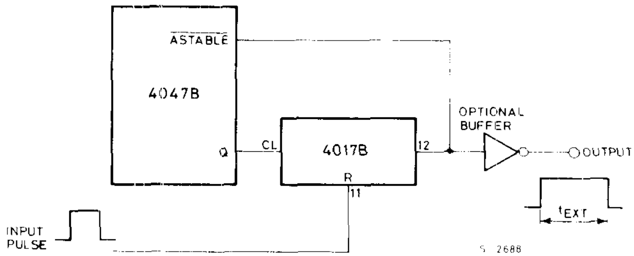
Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time.
A typical implementation is shown in Fig. B. The pulse duration at the output is

$$t_{ext} = (N - 1)(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

APPLICATION INFORMATION (continued)

Fig. B - Implementation of external counter option



6 - Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula:

Astable Mode: $P = 2CV^2f$. (Output at Pin 13)
$P = 4CV^2f$. (Output at Pin 10 and 11)

Monostable Mode: $P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$
(Output at Pin 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.
Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above).

7 - Timing-component limitations

The capacitor used in the circuit should be non-polarized and have low leakage(i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). Three is no upper or lower limit for either R or C value to maintain oscillation.
However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.
The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100$ pF, up to any practical value, for astable modes;
$C \geq 1000$ pF, up to any practical value, for monostable modes.
$10\ K\Omega \leq R \leq 1\ M\Omega$.