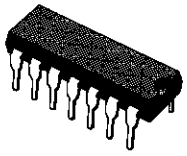
SGS-THOMSON MICROELECTRONICS

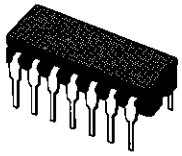
M54HCT10
M74HCT10

TRIPLE 3-INPUT NAND GATE

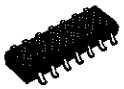
- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS10



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

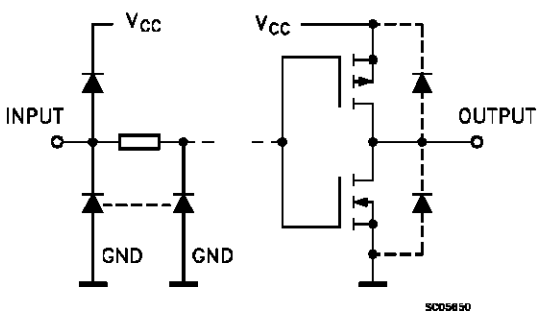
M54HCT10F1R	M74HCT10M1R
M74HCT10B1R	M74HCT10C1R

DESCRIPTION

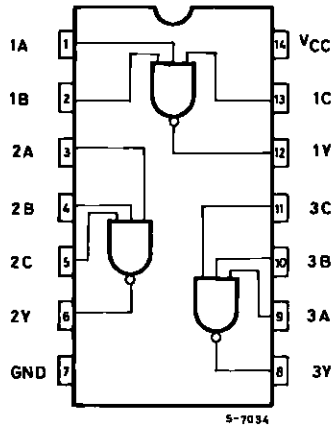
The M54/74HCT10 is a high speed CMOS TRIPLE 3-INPUT NAND GATE fabricated with silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

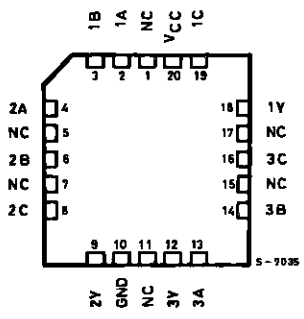
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



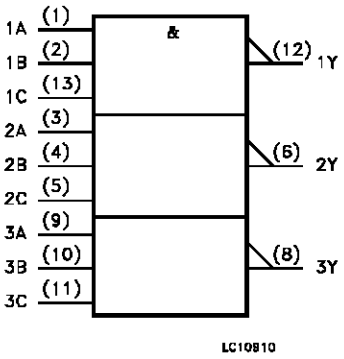


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

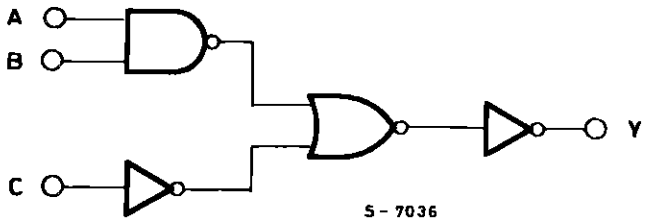
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	Data Inputs
2, 4, 10	1B to 3B	Data Inputs
13, 5, 11	1C to 3C	Data Inputs
12, 6, 8	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	^oC ^oC
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

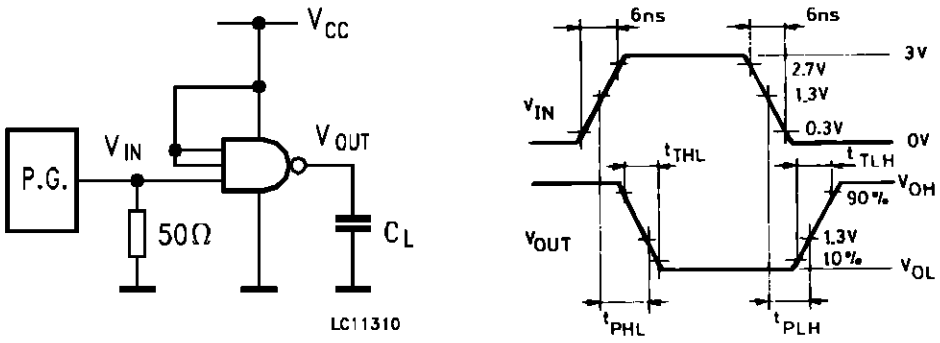
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 ^oC 54HC and 74HC			-40 to 85 ^oC 74HC		-55 to 125 ^oC 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

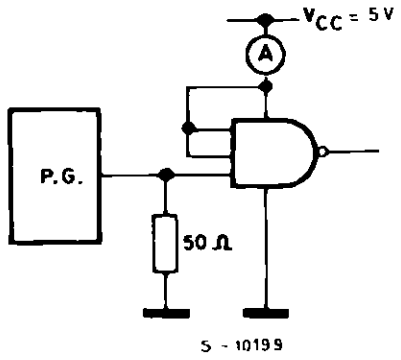
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			14	22		28		33	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				46						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.