PDP 7

PROGRAMMED DATA PROCESSOR — 7

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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PDP-7

1.75-microsecond core memory cycle

3.5 -microsecond add time

4.4-microsecond average high-speed multiply

9 -microsecond average high-speed division

8 auto indexing memory locations

10-megacycle silicon circuitry

18-bit parallel operations

36- or 18-bit arithmetic, fixed- or floating-point (programmed)

256 input/output stations, with program interrupt

4096- to 32,768-word core memory

570,000 word transfers per second

Extensive programming system, with FORTRAN II compiler

FORTRAN operating system for installations with Microtape

Computer-aided programming

Indirect (deferred) addressing

Input/output bus

Real-time control

Complete selection of input/output equipment

PDP-7 SYSTEM DESCRIPTION

The Programmed Data Processor-7 (PDP-7) is a multipurpose digital computer designed for engineering and scientific use in laboratories and computation centers. The standard system includes the processor, 4096-word core memory, real-time control, operating console, and input/output console typewriter for keyboard or perforated tape input and output. The standard programming system includes the Symbolic Assembler and Relocating Linking Loader, Symbolic Debugging Program, Symbolic Tape Editing Program, and FORTRAN II Compiler.

PROCESSOR

The processor performs logical and arithmetic functions, provides access to and from the memory, and controls the flow of data to and from the computer. It consists of the Process Controller, which issues timing, state, and other signals to other elements of the processor, and six active registers.

The ACCUMULATOR (AC) is an 18-bit register which performs arithmetic and logical operations on the data and acts as an input/output register to transfer data between memory and input/output stations. It can be cleared, complemented and shifted right or left with the Link.

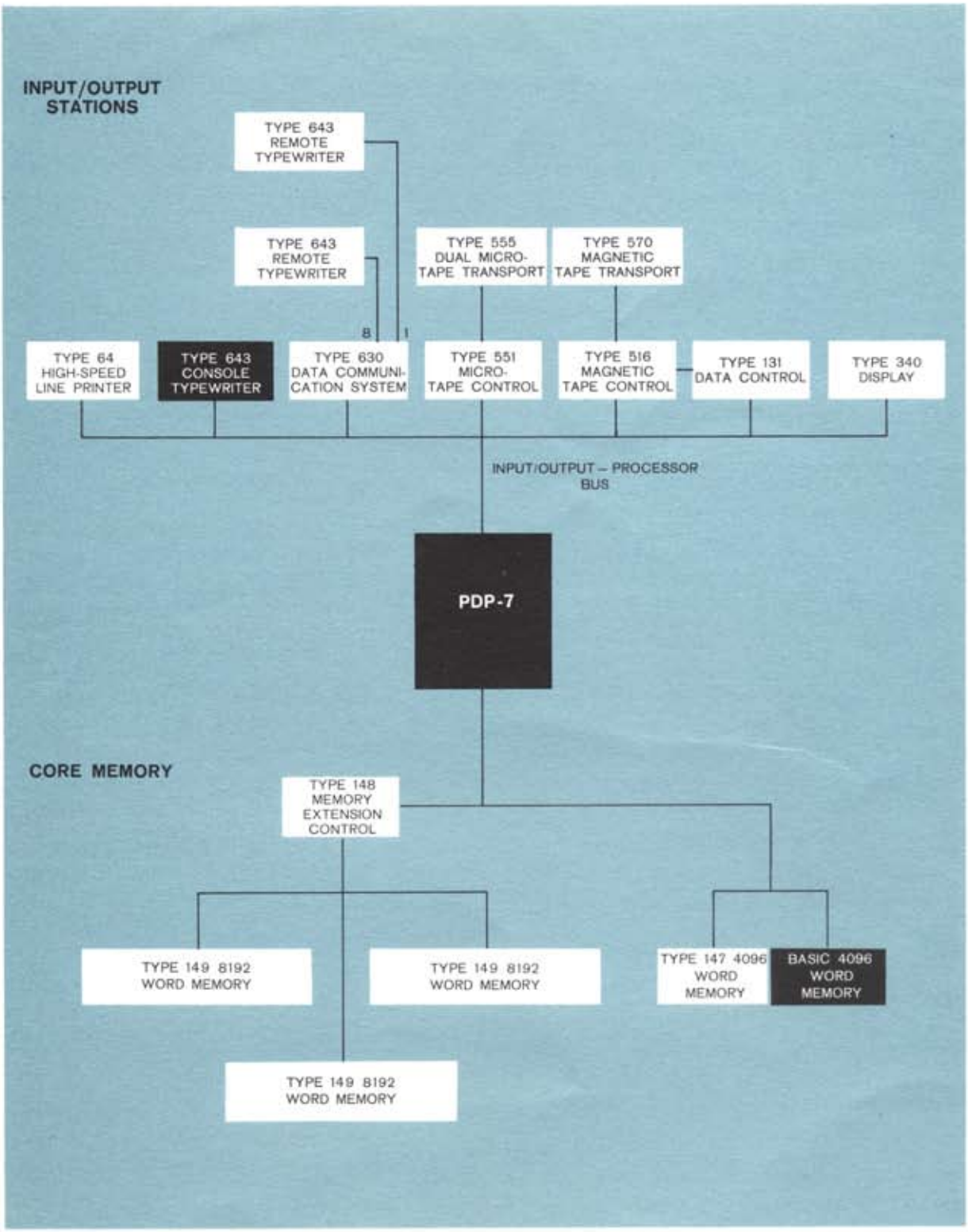
The LINK (L) is a 1-bit register used to extend the precision of the accumulator, permitting more rapid performance of 36-bit arithmetic and acting as the carry register for twos complement arithmetic. It can be cleared, complemented, and sensed.

The MEMORY ADDRESS REGISTER (MA) is a 13-bit register which holds the address of the core memory cell currently being used. The address can be deposited in the MA from the MEMORY BUFFER REGISTER, PROGRAM COUNTER, or an input/output station causing a data interrupt. The MA can be cleared or incremented by one.

The MEMORY BUFFER REGISTER (MB) is an 18-bit buffer which stores data and instructions temporarily as they are being transferred between memory and input/output stations, ACCUMULATOR, PROGRAM INSTRUCTION REGISTER, or PROGRAM COUNTER. The MB can be incremented by one.

The PROGRAM INSTRUCTION REGISTER (PIR) is a 4-bit register which holds the operation code of the program instruction currently being performed. The code is taken from the corresponding bits of the MEMORY BUFFER REGISTER.

The PROGRAM COUNTER (PC) is a 13-bit register which holds the address of the next memory cell from which an instruction is to be taken. The address of the next instruction can come from the MEMORY BUFFER or MEMORY ADDRESS REGISTERS or from the ADDRESS SWITCH REGISTER on the operating console.



PDP-7 SYSTEM DIAGRAM

MEMORY

The memory stores operands and instructions. In the basic system it consists of a single, 4096-word module which cycles in 1.75 microseconds, that is retrieves the number stored in the memory cell specified by the MEMORY ADDRESS REGISTER, writes the number into the MEMORY BUFFER REGISTER, and rewrites it into the same memory

REAL-TIME CONTROL

The Real-Time Control links up to 256 input/output stations by a bus to the processor, calls the stations, collects and distributes the input/output data, interrupts to perform the subroutines required by input data, interrupts for feeding data in or out, permits program instruction skipping based on the status of the input/output stations, and generates timing pulses.

The functions of the Real-Time Control are:

Input/output station calling — performed by decoders which read input/output transfer instructions, call the ' required station, test its status, and read data out or in.

Data collecting — accepts parallel input data from the station called by the input/output instruction and transfers it to the accumulator.

Data transmitting — transfers the data word in the accumulator to the proper input/output station.

Program interrupting — an operating mode which permits specified conditions of input/output stations to interrupt the program and initiate a subroutine to process data for or from the input/output station. The contents of the processor's registers are stored in memory while the interruption continues, then the program resumes when the subroutine is completed.

Data interrupting — an operating mode which allows the processor to interleave date transfers, at rates up to 570,000 words per second, with the operating program.

Input/output skipping — an operating mode which directs the program to skip input/output subroutines if the input/output station is not ready.

Real-time clock — provides a counting resolution of 16.6 milliseconds and can be preset to interrupt the program at predetermined intervals.

INPUT/OUTPUT

The console typewriter permits the operator to enter data into the processor on perforated paper tape or on the keyboard at 10 characters per second. Output from the processor, on perforated paper tape or printed, is also presented at 10 characters per second.

MEMORY SUBSYSTEM

The basic 4096-word PDP-7 memory can be expanded to 32,768 words using the Type 148 Memory Extension Control and the 8192-word Type 149 Memory Modules. Word length is 18 bits, and cycle time is 1.75 microseconds. Memory contents are not affected by power failure.

INPUT/OUTPUT SUBSYSTEM

The input/output subsystem includes the bus, real-time control, and up to 256 input/output stations. The bus consists of station selection, data, control, and status sensing lines. It simplifies expansion in the field, since new input/output stations need not be connected to the processor, only to the bus. An optional 16-channel, priority interrupt system signals the processor when an input/output station requires service. The processor can service most of the input/output stations simultaneously.

FAST, EASY MAINTENANCE

Three features of the PDP-7, in addition to the proven reliability of the System Modules from which it is built, insure fast, easy maintenance and a lower mean time to repair. These provisions are built-in marginal checking, a complete set of diagnostic programs and routines for the processor, memory, and input/output stations, and parallel organization to permit rapid isolation of error sources.

PROGRAMMING SYSTEM

The basic programming system for the PDP-7 includes the Symbolic Assembler and Relocating Linking Loader, Symbolic Debugging Program, Symbolic

Editing Program, the FORTRAN II Compiler with a standard FORTRAN library, Input/Output Programs, Arithmetic Routines, and utility and maintenance routines. All will operate in the basic PDP-7: processor, 4096-word memory, and Console Typewriter with paper tape punch and reader.

The programming system is designed to make fully available to each user the unlimited general-purpose computing ability of the PDP-7 and to serve as the operating nucleus of an extensive library of programs and routines to be made available to all installations. New techniques, routines, and programs are always being developed, field-tested, and documented in the Digital Program Library for incorporation in each user's system. All are intended to let the system operate more efficiently and to increase the ease with which it is programmed.

PROGRAM PREPARATION

In the basic system, the FORTRAN Compiler produces an output in assembly language which serves as the input to the Symbolic Assembler and Relocating Linking Loader.

The PDP-7 Extended FORTRAN Operating System for installations with Microtape permits one-pass program preparation. It accepts source language inputs from the typewriter, paper tape, or prestored on Microtape. A feature of the system is on-line (run-time) debugging in the source language. The system halts at run time, having prepared, assembled, and called everything needed except the input data.

SYMBOLIC ASSEMBLY SYSTEM

Elements of the PDP-7 Symbolic Assembly System are the Symbolic Assembler and Relocating Linking Loader, the Symbolic Debugging System, and the Symbolic Tape Editing Program.

The assembly system allows the programmer at any PDP-7 installation to work in a system context. A conditional assembly feature allows the selective assembly of master library subroutines, and a macro feature permits easy generation of a local or private library. If desired, the linking loader will produce at run time an absolute listing for the linked object programs.

Symbolic Debugging System DDT-7 lets the programmer use the PDP-7 to debug on-line at run time, giving him instantaneous feedback when he makes changes. This dynamic debugging, extensively developed by Digital, gives the user close control, preventing flaws in his object program from destroying significant portions of the memory contents. Using the typewriter, he can communicate conveniently with the PDP-7 in the symbols of his assembly language. He can control the execution of any portion of his object program by inserting breaks in it. When the computer reaches a break, it transfers control of the object program to DDT-7. The user can then examine and change the contents of individual memory registers to correct and refine his object program.

The Symbolic Tape Editor lets the user edit, correct, and update symbolic object program tapes using the PDP-7 and the console typewriter.

FORTRAN II COMPILER

Assembly languages are essentially oriented toward the machine, rather than toward the procedures for solving problems. The program written in assembly language has, accordingly, a close relationship to the machine language version of the program in number of instructions and in the degree to which the format of the machine instruction dictates the format of the symbolic language instruction. FORTRAN (for FORmula TRANslation) provides a language that is oriented instead toward the problem-solving procedures. It lets the programmer express the problem he is trying to solve in a mixture of English words and mathematical statements that is close to the language of mathematics and is also intelligible to the computer. In addition to shortening the time needed to prepare programs, it lets the user with little or no knowledge of

the computer's organization and machine language write effective programs for it.

The FORTRAN language consists of four general types of statements: arithmetic, logic, control, and input/output. It permits the use of fixed- and floating-point constants, variable names, subscripts, functions and subroutines not in the FORTRAN library, and several types of input/output equipment.

The FORTRAN II Compiler for the PDP-7 contains the instructions the computer needs to carry out the clerical work of translating the FORTRAN version of the problem statement into an object program in machine language. It also produces diagnostic messages to help pinpoint source language errors. After a program is compiled with FORTRAN, it and the data it will work with are loaded into the computer to solve the problem. Sin, cos, square root, natural log, exponential, arctan, and absolute value are the standard library subroutines supplied.

INPUT/OUTPUT PROGRAMS

The input/output programs for the PDP-7 include a magnetic tape package for conventional magnetic tape installations, a Microtape package for use with the Microtape Dual Transport and Control System, routines for using Precision Displays and Light Pens, and a buffered input/output package to permit simultaneous use of the typewriter, high-speed paper tape reader, tape punch, card reader, card punch, and line printer.

ARITHMETIC ROUTINES

Arithmetic routines include fixed- and floating-point double precision packages, multiply and divide subroutines, automatic multiplication and division with the Extended Arithmetic Element, and standard elementary function subroutines.

UTILITY AND MAINTENANCE ROUTINES

Other routines are provided for duplicating and verifying tapes, testing basic machine functions, testing machine instructions, testing memory, and testing the typewriter. Routines to test optional input/output equipment are provided with the equipment.

TRAINING AND ASSISTANCE

Digital offers monthly courses in programming and maintaining each of its computer models as part of the service provided to purchasers. These courses include instruction by experienced Digital personnel, training manuals, and supplies. Classes are kept small to insure adequate individual attention. Digital will assist you with specific programming problems before, during, and after installation of your computer and can provide a computer at our home office to let you check out your programs under the guidance of Digital programmers until your own computer is on line.

DECUS LIBRARY AND NEWSLETTER

In addition to the Digital PDP-7 Program Library, users of Digital equipment have access to the growing DECUS Library of utility programs, subroutines, and other programming materials. DECUS (for Digital Equipment Computer Users' Society) was formed to promote a free and effective interchange of information. A principal channel for the information flow is DECUSCOPE, a monthly technical newsletter to which users contribute their ideas, techniques, routines, and program summaries. The DECUS Library distributes to members program write-ups and the corresponding program tapes and listings. Certification of these materials is under the direction of the users' programming committee, which also guides the operation of the Library. DECUS also publishes the proceedings of its annual symposiums and frequent seminars.

The operating console is designed to simplify and speed programming, operation and maintenance of the PDP-7. It includes keys and switches to start and stop the computer, examine the contents of any memory register and any processor register, deposit words in memory, turn the power on and off, and step through the program at variable speeds. The complete array of indicators permits the operator to determine the state of every active register in the computer.

PDP-7 INSTRUCTIONS

MEMORY REFERENCE INSTRUCTIONS

Addressable or memory reference instructions which contain a memory address. The address portion of the instruction word specifies the location of an operand in the memory.

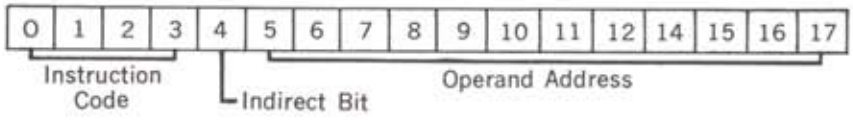
Mnemonic Code	Octal Code	Time (μsec)	Operation
cal	00	3.5	Same as jms 20. The address portion of this instruction is ignored. The cal instruction may be used for calling subroutines via a master central program which keeps track of exit addresses, allocates storage, and supplies parameters to the subroutines.
dac Y	04	3.5	Deposit Accumulator. C(AC)* are deposited in memory register Y. The C(AC) are unaffected by this operation.
jms Y	10	3.5	Jump to Subroutine. C(PC) are deposited in memory register Y. The next instruction will be taken from Y + 1, the beginning of the subroutine.
dzm Y	14	3.5	Deposit zero in memory. The contents of register Y are changed to zero. The original contents of Y are lost.
lac Y	20	3.5	Load AC. The C(Y) replace the C(AC). The previous C(AC) are lost. The C(Y) are unaffected.
xor Y	24	3.5	Exclusive OR. The exclusive "OR" logical function is performed on a bit-by-bit basis between the C(AC) and C(Y). The result is left in the AC and the original C(AC) are lost.
add Y	30	3.5	Add (ONE's Complement). The C(Y) are added to the C(AC) in ONE's complement arithmetic. The result is left in the AC and the original C(AC) is lost. This type add instruction is commonly used for most arithmetic. The Link bit is set to a ONE if the sum of the magnitude of C(Y) and C(AC) is greater than $2^{17} - 1$.
tad Y	34	3.5	Add (TWO's Complement). The C(Y) are added to C(AC) in TWO's complement arithmetic. If there is a carry out of bit 0, the Link will be set to ONE. This type of add instruction is useful in multiple precision arithmetic.
xct Y	40	1.75+ instruction execute time	The instruction in register Y will be executed. The computer will act as if the instruction located in Y were in the place of the xct Y.
isz Y	44	3.5	Index and Skip if zero. The C(Y) are replaced by C(Y) + 1. The C(AC) are unaffected by this instruction. The addition is done using two's complement arithmetic. If the sum is +0, the next instruction is skipped.
and Y	50	3.5	Logical AND. The logical "AND" function is performed on a bit-by-bit basis between C(AC) and C(Y). The result is left in the AC and the original C(AC) are lost.
sad Y	54	3.5	C(Y) are compared with the C(AC). If the two numbers are different, the next instruction in the sequence is skipped. The C(AC) and C(Y) are both unaffected by the instruction.
jmp Y	60	1.75	Jump. The C(PC) are reset to address Y. The next instruction to be executed is taken from memory register Y. The original contents of the PC are lost.

* C(AC): contents of the accumulator.

PROGRAMMING

The PDP-7 uses two types of instructions: memory reference and augmented. Memory reference instructions store or retrieve the data they use in core memory. Augmented instructions do not store or retrieve data in memory. They let the programmer use the address portion of the instruction to specify logical operations, giving the PDP-7 a microprogramming capability. Instruction execution times are multiples of the1.75-microsecond core memory cycle time. Memory reference instructions are carried out in 1.75 or 3.5 microseconds, with an additional 1.75microseconds required for single-level indirect addressing. Augmented instructions are carried out in 1.75 microseconds.

The instruction word format is shown below. The first four bits contain the code of the instruction to be performed. The fourth bit, when it contains a one, instructs the computer to use the indirect, or deferred, address selection mode. In this mode, the computer finds in the memory location specified by the address portion a 13-bit actual address in which to retrieve or store the data it needs or is working with. If the memory location containing the actual address is one of the auto indexing registers, 10_8 through 17_8, a one is added to the number before it is used for the address. This lets the computer perform many addressing functions for the programmer.



AUGMENTED INSTRUCTIONS

Augmented instructions provide micro programming capability by using the address portion of the instruction to select logical operations. These instructions do not address a memory register.

The following instruction loads itself into the AC.

Mnemonic Code	Octal Code	Time (μsec)	Operation
law	76	1.75	The address position of this instruction may be used to specify a constant.

OPERATE GROUP

The operate instructions use bits 5 through 17 to specify variations of the basic instructions.

Mnemonic Code	Octal Code	Time (μsec)	Operation
opr	74xxxx	1.75	Operate. The operate instruction is also the conditioning (skip) instruction. When a particular condition is present, the following instruction will be skipped. The various micro program events occur at different times to allow several events to be programmed which affect the same element. This is a micro program instruction using bits 4-17 to specify the desired operations. Combinations of the individual operations can be made. The operations are specified by bits as follows

Mnemonic Code	Octal Code	Operation	Sequence of Occurrence
cma	1	Complement AC.	3
cml	2	Complement Link.	3
oas	4	Inclusive OR AC switches with AC.	3
ral	10	Rotate AC and Link left one place.	3
rtl	2010	Rotate AC and Link two places left.	2, 3
rar	20	Rotate AC and Link right one place.	3
rtr	2020	Rotate AC and Link two places right.	2, 3
hlt	40	Halt the machine	4
sma	100	Skip on minus AC. If $AC_0 = 1$, the next instruction in sequence is skipped.	1
spa	1100	Skip on plus AC. If $AC_0 = 0$, the next instruction in sequence is skipped.	1
sza	200	Skip if AC ≠ 0.	1
sna	1200	Skip if AC ‡ 0.	1
snl	400	Skip if Link ‡ 0.	1
szl	1400	Skip if Link ≠ 0.	1
skp	1000	Skip unconditionally.	1
cll	4000	Clear Link.	2
cla	10000	Clear AC.	2

IN-OUT TRANSFER GROUP

The instructions in this group are similar to the Operate Group instructions except they pertain to the transfer of information between the Central Processor and various input-output devices. Bits 4 through 17 select and control input-output devices.

Mnemonic Code	Octal Code	Time (μsec)	Operation
iot	70xxxx	1.75	In Out Transfer. This instruction which forms a micro program is used to select an input or output device. The instruction forms a micro program and has the following format:

Function	Command Bits
Specifies the in-out instruction (Operation Code 1110)	0-3
May be used to select sub-device	4-5
Selects the device	6-11
May be used to select sub-device	12-13
Clears the AC at event time 1 if a ONE	14
Transfers an IOT pulse at event time 3 if a ONE	15
Transfers an IOT pulse at event time 2 if a ONE	16
Transfers an IOT pulse at event time 1 if a ONE	17

Bits 13-17 may be used together in any combination to allow various types of in-out command structures, and these may handle 1, 2, or 3 devices per selection (bits 4-12) depending upon the requirements of the devices.

OPTIONAL EQUIPMENT

CENTRAL PROCESSOR OPTIONS

CORE MEMORY MODULE TYPE 147

Extends PDP-7 core memory by 4096 words.

CORE MEMORY EXTENSION CONTROL TYPE 148

Allows memory extension from 8192 to 32,768 words.

CORE MEMORY MODULE TYPE 149

Extends core memory by 8192 words.

EXTENDED ARITHMETIC ELEMENT TYPE 177

Adds 23 microcoded instructions including automatic multiply, divide, normalizing, and long shifting.

BLOCK TRANSFER DRUM SYSTEM TYPE 24

Drum transfers operate through the computer's data interrupt facility permitting interlaced program and drum transfer operation.

Type 24E	32,768 words
Type 24F	65,536 words
Type 24G	131,072 words

AUTOMATIC PRIORITY PROGRAM INTERRUPT TYPE 172

Provides 16 levels of priority program interrupt, each associated with a unique location in memory. Includes individual channel enable/disable register.

DISPLAY OPTIONS

PRECISION CRT DISPLAY TYPE 30D

Plots data point by point on a 16-inch cathode ray tube. Separately variable 10-bit X and Y coordinates. Includes program intensity control.

PRECISION INCREMENTAL CRT DISPLAY TYPE 340

Plots points, lines, vectors, and characters on a 9⅜-inch-square raster of 1,024 points along each axis. Plotting rate is 1½ microseconds per point in vector, increment, and character modes. Random point plotting rate is 35 microseconds.

HIGH SPEED LIGHT PEN TYPE 370

Uses fiber optic light pipe and photomultiplier system for fast detection of displayed information.

OSCILLOSCOPE DISPLAY TYPE 34

Plots data point by point on an X-Y plotting scope such as the Tektronix Model RM 503. Ten bits per axis.

INCREMENTAL PLOTTER AND CONTROL TYPE 350

With Model 560. 12-inch paper; 12,000 steps per minute.

With Model 565. 12-inch paper; 18,000 steps per minute.

With Model 563. 31-inch paper; 12,000 steps per minute.

With Model 564. 31-inch paper; 18,000 steps per minute.

PAPER TAPE AND CARD EQUIPMENT

CARD READER AND CONTROL TYPE 421A

Provides on-line reading of up to 200 standard punched cards per minute in either alphanumeric or binary mode.

CARD READER AND CONTROL TYPE 421B

Same as 421A except 800 cards per minute.

CARD PUNCH CONTROL TYPE 40

Controls 100 card-per-minute IBM 523 Summary Punch. Buffer holds one 80-bit row

PERFORATED TAPE PUNCH AND CONTROL TYPE 75

Punches 5, 7 or 8-hole tape at 63.3 cps.

PRINTERS

AUTOMATIC LINE PRINTER AND CONTROL TYPE 64

Prints 300 lines per minute, 120 columns per line, 64 characters per column. Includes single line 120 character buffer.

DATA COMMUNICATION SYSTEM TYPE 630

Provides interface for up to 64 remote typewriter stations for multi-user on-line inputs and outputs.

MAGNETIC TAPE EQUIPMENT

AUTOMATIC MAGNETIC TAPE CONTROL TYPE 57A

Controls up to eight tape transports automatically. Provides information transfer through computer's data interrupt facility, permitting interlaced program and tape operation. Controls reading or writing of tape at various rates compatible with IBM, BCD or binary parity modes.

MAGNETIC TAPE TRANSPORT TYPE 570

Reads and writes IBM formats on ½ inch tape at transfer rates from 15-62.5 KC. Tape speed is 75 or 112.5 ips with densities of 200 or 556 bits per inch.

MAGNETIC TAPE TRANSPORT TYPE 50

Reads and writes IBM-compatible magnetic tape at transfer rates of 15,000 or, 41,700 cps, and 200 or 556 bpi.

DUAL MICROTAPE SYSTEM

Provides a fixed address magnetic tape facility for high speed loading, readout and program updating.

Type 555 Dual Transport Includes two independent tape drives

Type 550A Control Unit Controls up to 4 Type 555 Dual Tape Transports

IN-OUT CONNECTIONS AND CONTROLS

18-BIT OUTPUT RELAY BUFFER TYPE 140

18 spdt relays actuated by computer command.

DATA CONTROL TYPE 174

Controls and double buffers high speed transfer between the computer and external devices at word rates to 570 KC.

DATA INTERRUPT MULTIPLEXER TYPE 173

Provides multiplex control for simultaneous operation of three high-speed devices such as the Type 57A Tape Control, Type 24 Drum, etc. Maximum combined transfer rate: 570,000 18-bit words per second.

ANALOG-TO-DIGITAL EQUIPMENT

GENERAL PURPOSE A-D CONVERTER TYPE 138

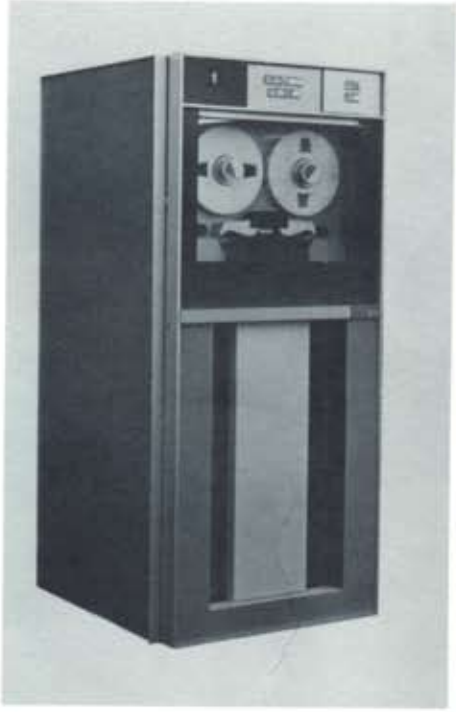
Used to convert input analog voltages into digital numbers for computer entry. Conversion time varies from 9 to 88 microseconds, depending upon accuracy and resolution desired.

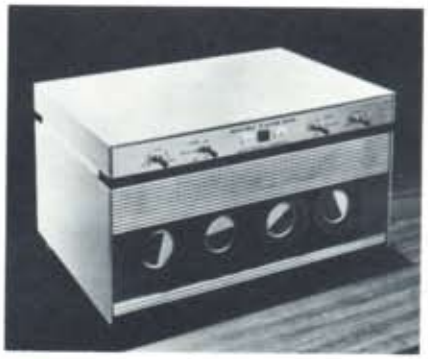
GENERAL PURPOSE 64 CHANNEL MULTIPLEXER CONTROL TYPE 139

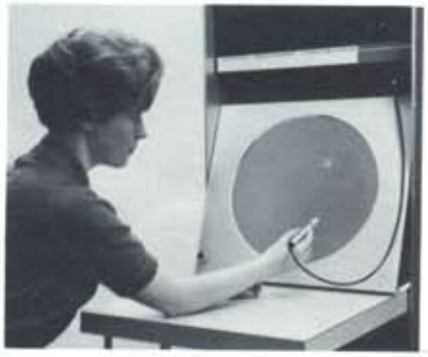
Controls up to 64 channels of analog input to be multiplexed into the analog to digital converter.

HIGH SPEED A-D CONVERTER TYPE 142

Converts analog signals to digital information with 10-bit accuracies in 5 microseconds for computer entry.







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